

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket Number 15150US01

In re Application of:)	
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Hatti)	
)	Electronically Filed
Serial No.: 10/799,032)	
)	On: March 24, 2009
Filing Date: 3/12/2004)	
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Examiner: Findley)	
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Confirmation No.: 6706)	
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Group Art Unit No. 2621)	
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REQUEST FOR PRE-APPEAL REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This amendment is filed in response to the Office Action of
12/24/08.

REMARKS

Claims 1, 2, 4-6, and 8-12 are presently pending. Assignee respectfully requests pre-appeal review of the rejections to claims 9 and 11.

Claim 9 was rejected under 35 U.S.C. § 102(b) as being anticipated by Baden. Claim 11 recites, among other limitations, "fetching a portion of a picture stored in a frame buffer, the portion of the picture being stored with a pixel order" and "storing the portion of the picture in another buffer with the predetermined pixel order".

Examiner has made reference to Baden, Figure 6, references 623 and 625; column 15, line 64 - col. 16, line 4, Figs 2A, 2B. Assignee traversed and noted that none of the foregoing describe that "fetching a portion of a picture stored *in a frame buffer*, the portion of the picture being stored with a pixel order" and "storing the portion of the picture in *another buffer* with the predetermined pixel order".

In response, Examiner has argued that "Baden discloses that Fig. 6 corresponds to the bridge/graphics controller 311 of Fig. 3, wherein the bridge/graphics controller 311 is connected to main memory subsystem 309 via a data bus 305. Accordingly, data bus 305 functions as the input to the schematic illustrated in Fig. 6 of Baden, and, therefore, main memory subsystem may be considered a frame buffer. Consequently, flip flop 625 of Fig. 6 in Baden may be considered a buffer that stores the pixels in the predetermined order, since flip flop 625 immediately follows the byte-swap mux 649."

Assignee maintains traverse. It is noted that in Figure 6, the input path to the flip flop 625 comes from the System Data Bus 305, connecting the Bridge/Graphics

Controller 311 to the processor 307. Although Examiner argues that "memory subsystem may be considered a frame buffer", there is absolutely no teaching in Baden that memory subsystem 309 stores a picture. Assignee notes that it is well established law that for anticipation, the reference must expressly or inherently teach each of the claimed limitations. Accordingly, even if the "frame buffer" is deemed "memory subsystem 309", "a *picture stored in a frame buffer*" cannot be read onto memory subsystem.

Furthermore, although Haden teaches that "An image to be displayed is stored in a frame buffer 317", flip flop 625 does not receive input from the frame buffer 317 (see Figure 6). Accordingly, Baden does not teach "fetching a portion of a picture stored *in a frame buffer*, the portion of the picture being stored with a pixel order".

Accordingly, Assignee respectfully traverses the rejection to claims 9 and 11. Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claims 9-12.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully requests that the rejections to claims 9-12 be reversed. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: March 24, 2009

Respectfully submitted,



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